On the Comparison of Synchronous versus Asynchronous Circuits under the Scope of Conducted Power-Supply Noise

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***Abstract*— Nowadays, the major part of electronic devices make use of synchronous circuits controlled by a global clock signal. However, the noise sensitivity as well as the electromagnetic emission of this type of circuit is very high. In this context, asynchronous circuits represent a very interesting solution, since they are naturally more robust than the synchronous counterparts. The proposed work aims at comparing the robustness of synchronous and asynchronous circuits generated according to the Desynchronization Approach presented in [1] when they are exposed to power supply disturbances (PSD). To provide the necessary results to compare the two different design paradigms, we performed a set of experiments according to the IEC 61.000-4-17 and the IEC 61.000-4-29 Normatives [2,3]. The obtained results demonstrate that the asynchronous circuit is significantly more robust than the synchronous one.**

I. INTRODUCTION

Technology scaling has made possible the integration of millions of transistors into a small area, automatically decreasing the gate delay and consequently increasing the operating frequencies of the circuits. However, these enhancements have also introduced other critical issues related to their reliability and power consumption. Modern integrated circuits are usually implemented exploiting the synchronous paradigm where a global clock signal controls the entire circuit. Despite the great dissemination of this paradigm, synchronous circuits introduce critical constrains with respect to their very high noise sensitivity, high electromagnetic emission as well as power consumption. In this scenario, the asynchronous paradigm has been proposed as an interesting solution able to provide intrinsically more robust and low power circuits [4]. In more detail, asynchronous circuits can operate reliably at very low voltages and can save even more power since they naturally perform computation *on-demand*. Indeed, asynchronous circuits provide other important advantage, because they reduce the electromagnetic emission.

The increasing hostility of the electromagnetic environment, caused substantially by the ubiquitous adoption of wireless technologies as mobile electronics, represents a huge challenge for the reliability of real-time embedded systems [5]. In detail, external conditions like Electromagnetic Interference (EMI) and Power Supply Disturbance (PSD) can generate transient faults that tend to disappear rapidly [6]. For critical applications running on low-power, battery-supplied embedded electronics, PSD represents one of the most common sources of transient faults.

In this scenario, paper proposes to compare the robustness of the synchronous and asynchronous circuits when exposed to PSDs. In order to obtain the necessary information to compare the two types of implementations, we implemented a case study using a DLX processor [9]. Fault injection experiments have been performed based on the IEC 61.000-4-17 and IEC 61.000-4-29 normatives in order to determine the electromagnetic susceptibility of the two different design paradigms.

The paper has been organized as follows: *Section II* summarizes a previous work, where synchronous and asynchronous paradigms were compared in terms of electromagnetic emissions and susceptibility. In *Section III* we describe the case study adopted, presenting the synchronous and asynchronous implementations of the DLX processor. *Section IV* presents the experimental results emphasizing the fault injection environment developed and the obtained results. Finally, in *Section V* we draw the conclusions.

II. BACKGROUND

Asynchronous designs have recently received increased attention due to their low electromagnetic noise emission as well as power consumption. In particular, this type of circuit represents a very interesting solution to mission-critical applications, wherein reliability is a key [7].

In this scenario, a previous work compared synchronous and asynchronous circuits [8]. This paper presents the first concrete evaluation of the Quasi Delay Insensitive (QDI) asynchronous logic in terms of Electromagnetic Compatibility (EMC). Indeed, the paper adopts a case study based on a Data Encryption Standard (DES) crypto processor and provides a comparison between its synchronous and asynchronous versions.

Regarding the electromagnetic emission, the published results demonstrate that the power emission of the asynchronous version of the DES crypto processor is 5.6 times lower than its synchronous counterpart, knowing that the asynchronous circuit is 27 times faster than the synchronous one.

Moreover, both circuits have been also evaluated in terms of conducted immunity applying a sinusoidal signal to the power supply pads. Considering an operating frequency below 200 MHz, the susceptibility of both circuits is quasi identical. However, when the operating frequency increases, the sensitivity of the asynchronous circuit is much lower than the sensitivity of the synchronous one. In fact, the power needed to disturb the asynchronous DES crypto processor has to be 10 times higher than the one necessary to corrupt the synchronous circuit.

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Although the novelty of the previously described work [8], it is important to note that one of the major drawbacks of asynchronous circuits is the *high design complexity*, as it is also the case for Quasi Delay Insensitive (QDI) asynchronous logic. In this sense, the present work addresses this problem by introducing the Desynchronization Approach [1] as a possible solution to minimize the asynchronous circuits design complexity. Having this in mind, we present hereafter a behaviour analysis of this type of circuit architecture with regards to the conducted electromagnetic immunity, by taking as reference the synchronous version of such architecture. Moreover, no IEC Normative guided the experiments performed in [8] in order to analyse the conducted immunity of the circuits. If we think from the point of view of *experiment reproducibility*, the use of IEC Normatives is recommended if one desires to repeat experiments to check results validity or compare with different approaches.

III. CASE STUDY

To conduct the robustness comparison between synchronous and asynchronous circuits when exposed to PSD, we adopted a case study composed of the synchronous and asynchronous versions of the DLX processor [9]. In this section we summarize the main characteristics of the two versions of the targeted processor, as well as the Desynchronization Approach used to produce the asynchronous version.

A. The Circuits

The developed case study adopts the synchronous and asynchronous versions of the DLX processor, called **AS**ynchronous o**P**en-source Processor **I**p of the **D**lx **A**rchitecture (ASPIDA) [10]. The DLX processor is a 32-bit 5-stage pipelined RISC CPU architecture. The DLX's pipeline implements the following states: (1) Instruction Fetch (IF), (2) Instruction Decode (ID), (3) Execute (E), (4) Memory (MEM) and (5) Write Back (WB). Fig. 1 shows the functional block diagram of the DLX processor.

The synchronous version adopted, named *Synchronous ASPIDA DLX*, supports the full DLX integer ISA and contains two memory interfaces, following the original DLX model, which supports byte, half-word and word transfers.

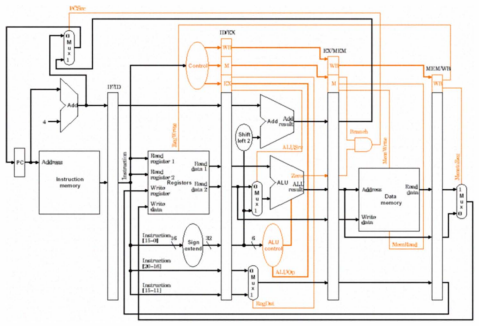

Fig. 1. Block diagram of the synchronous DLX processor.

The *Asynchronous ASPIDA DLX* has been generated applying the Desynchronization Approach presented in [1]. The essential idea behind this approach is to start from the synchronous synthesized circuit and directly replace the global clock network with a set of local handshaking circuits. The circuit is then implemented with standard tools, using the design flow originally developed for synchronous circuits. In this context, the only modification is the clock tree generation algorithm. In detail, the Desynchronization Approach assumes that the circuit works with the same clock edge and is composed of combinational blocks (CL) and registers implemented with D flip-flops (FF). Fig. 2 shows the asynchronous circuit generated from its synchronous version according to the Desynchronization Approach. This approach is divided in three main steps: First of all, the flip-flop-based synchronous circuit is converted into a latch-based one (*M* and *S* latches in Fig 2(b)). Afterwards, the matched delays for the CL are generated (denoted by rounded rectangles in Fig. 2(b)). Finally, the local controllers are implemented and interconnected in order to provide the local clocks (denoted as *Cntr* in Fig 2(b)). Due the space limitation, the local controllers will not be fully described herein. For further information, interested readers can address reference [1].

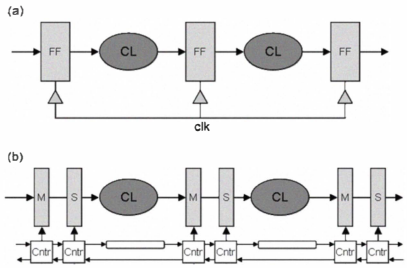

Fig. 2. Desynchronization Approach: **(a)** Synchronous circuit; **(b)** desynchronized version [1].

It is important to highlight that the essential novelty of this approach is that it provides a fully automated synthesis flow and it does not require any knowledge of asynchronous design. Therefore, the Desynchronization Approach incorporates *asynchrony* in a conventional EDA flow, without changing the "synchronous mentality" or requiring any new tool [1].

Fig. 3 shows the block diagram of the asynchronous ASPIDA DLX used. To generate the ASPIDA DLX, the DLX has been desynchronized according to [1]. In detail, the global clock signal has been removed and replaced by handshaking controllers. Afterwards, the flip-flops have been replaced by pairs of latches. Thus, observing Fig. 3 it is possible to see that the latches separating the datapath stages are locally clocked by controllers. These controllers are in charge of producing the appropriate signals to assure that the data move safely from one pipeline stage to the next one.

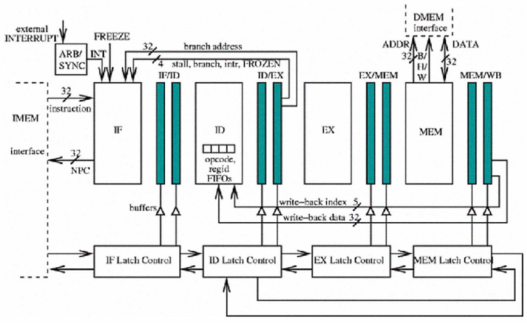

Fig. 3. Block diagram of the asynchronous ASPIDA DLX processor.

IV. EXPERIMENTAL RESULTS

In this section, we present the fault injection environment used and the results obtained during the experiments performed according to the IEC 61.000-4-17 and IEC 61.000-4-29 Normatives[1] [2,3].

[1] *The International Standard IEC 61.000-4-29 defines rules for injecting voltage dips, short interruptions and voltage variations on the Vdd/Gnd power lines, whereas the IEC 61.000-4-17 provides procedures for ripple injection on such lines.*

A. *Fault Injection Setup*

To provide the necessary results in order to compare the robustness of the two different design paradigms, we developed a fault injection environment, which included the following functional blocks:

- FPGA_0: it contains the synchronous version of the DLX processor.
- FPGA_1: it contains the asynchronous version of the DLX processor obtained applying the Desynchronization Approach.
- FPGA_clk: it contains the (50MHz) clock generator logic, which provides reference signal to both synchronous and asynchronous versions.
- Power-Supply Disruption (PSD) Generator: it generates the power supply noise according to the above mentioned IEC normatives.

Fig. 4 summarizes the fault injection environment used to perform the experiments.

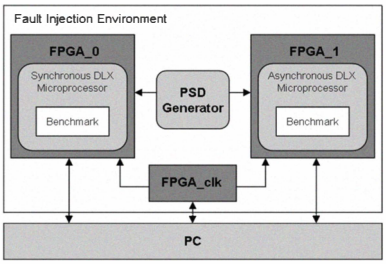

Fig. 4. Fault injection environment.

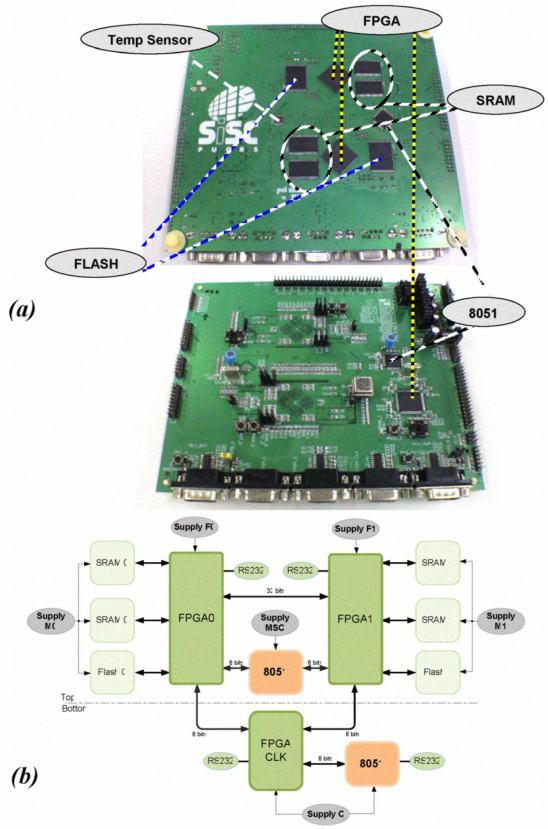

Fig. 5. IEC-compliant test board used to prototype the DLX processor versions: ***(a)*** General view; ***(b)*** Block diagram.

The fault injection environment was basically composed of three parts:

i) a six-layer board (see Fig. 5) specially designed to support conducted electromagnetic (EM) immunity measurements oriented by the IEC 61.000-4-17 and 61.000-4-29 Normatives. This board contains FPGA_1, FPGA_2 and FPGA_clk. One important characteristic of this board concerns the power supply lines, which were individually routed for each of the FPGAs, microcontroller and memories. This feature allows to control and inject noise into any of the onboard ICs or combination of them through dedicated power busses. Among the facilities available in this board, there is also a temperature sensor that allows one to perform a burn-in test in conjunction with IEC test sessions.

ii) a home-tailored board hosting the conducted power-supply noise generator logic (PSD Generator, Fig. 4).

iii) a personal computer (PC) used as test master controller.

The two versions of the DLX processor run a benchmark that execute the multiplication of two *10x10* matrixes. The experiment total time was around 20 hours. Fault injection campaigns have been performed according to the flow diagram depicted in Fig. 6.

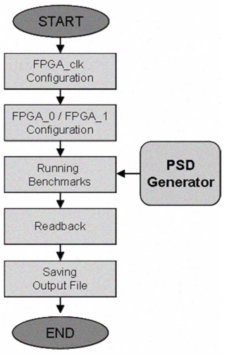

Fig. 6. Fault injection flow.

Figs. 7 and 8 display the IEC normative-compliant injected noise captured with oscilloscope at the *Vdd* input pins of FPGA_0 and FPGA_1. Noise was injected only at the core logic input pins of these devices, whose nominal voltage is 1.2 Volts, as defined by the fabricant. In both experiments noise was injected at a frequency of 32 KHz. It is worth to mention that the FPGAs periphery (I/O pads) remained at their nominal voltage levels: 3.3 Volts and 2.5 Volts during the whole experiment, since no noise was injected at these nodes.

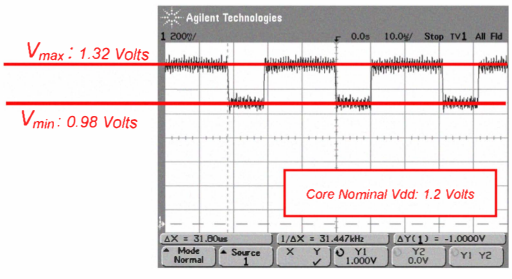

Fig. 7. IEC 61.000-4-17-compliant ripple injected noise captured with oscilloscope at the *Vdd* input pins of devices FPGA_0 and FPGA_1.

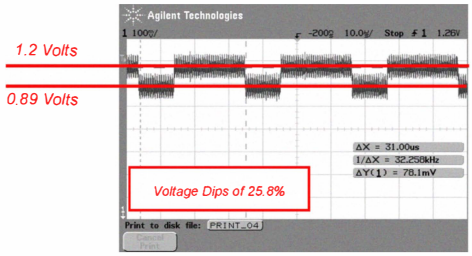

Fig. 8. IEC 61.000-4-29-compliant voltage dips captured with oscilloscope at the *Vdd* input pins of devices FPGA_0 and FPGA_1.

B. Results' Discussion

Fault injection experiments have been performed to generate the necessary information to compare the robustness of the two different design paradigms. With this goal in mind, a preliminary experiment was performed to evaluate the susceptibility of the two design paradigms to *power supply* decreases, by applying a negative *Vdd ramp* at the power supply pins of FPGA_0 and FPGA_1. In detail, we decreased step-by-step from 1.2 Volts the nominal *Vdd* of FPGA_0 and FPGA_1 till observing an erroneous output. The obtained results demonstrated that the asynchronous version is more robust than the synchronous one, since it remains operating properly until the nominal *Vdd* of 0.60 Volts, instead of 0.94 Volts of the synchronous version.

Next, Figs. 9 and 10 depict the results obtained during the experiments performed according to the IEC 61.000-4-17 and IEC 61.000-4-29 respectively.

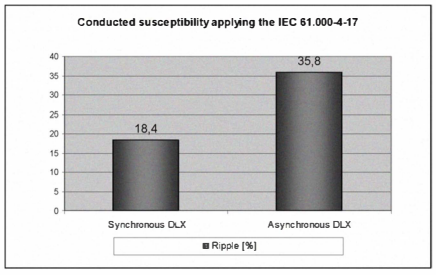

Fig. 9. Results obtained applying IEC 61.000-4-17.

Fig. 9 shows that the asynchronous DLX processor is clearly more robust than its synchronous counterpart, since it is able to support a nominal ripple on *Vdd* of 35.8% in comparison to only 18.4% for the synchronous DLX.

Observing Fig. 10, it is possible to conclude that the DLX processor asynchronous version is more robust than its synchronous counterpart, since it supports voltage dips until 52.1% with respect to the nominal *Vdd* of 1.2V, while the synchronous version supports voltage dips not larger than 25.6%.

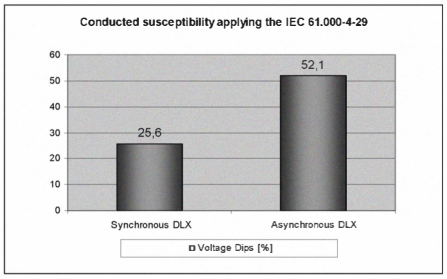

Fig. 10. Results obtained applying IEC 61.000-4-29.

V. Conclusions

In this paper we compared the robustness of synchronous and asynchronous circuits when exposed to noise conducted through power supply lines. With this purpose, we adopted a case study composed of the synchronous and asynchronous versions of the DLX processor. The asynchronous implementation of the processor was carried out according to an Approach named *Desynchronization*.

To compare the two design paradigms, we performed a set of practical experiments according to the following IEC normatives: 61.000-4-17 (for testing and measurement of ripple on the *Vdd* input pins) and the 61.000-4-29 (for voltage dips on the same pins). The obtained results demonstrate that the asynchronous circuit is significantly more robust than its synchronous counterpart.

In detail, the asynchronous DLX implementation is twice more robust than its synchronous version for the ripple injection experiment (since it was able to support a nominal ripple on *Vdd* of 35.8% in comparison to only 18.4% for the synchronous DLX). The same conclusion can be taken for the voltage dips applied to the *Vdd* input port, since the asynchronous version supported voltage dips of up to 52.1% with respect to the nominal *Vdd* of 1.2V, while the synchronous DLX implementation tolerated voltage dips not larger than 25.6%. Moreover, we applied a negative voltage ramp at the *Vdd* input port of both processor implementations and the obtained results indicated that the asynchronous version tolerated up to 50% [1-(0.6V/1.2V)] reduction on power supply lines against only 21.67% [(1–(0.94V/1.2V)] for the synchronous DLX architecture. In this case, the asynchronous implementation rendered the DLX processor roughly 2.3 times more robust to *Vdd* degradations than its synchronous counterpart.

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